ABSTRACT OF THE DISCLOSURE

A plurality of delay circuits successively delay a received data. The received data and delayed data signals are sampled in response to both leading and trailing edges of a clock having a frequency substantially identical with that of a data transmission rate of the received data. When a sampling value having the same value V (V=1 or 0) appears continuously N times in the sampling operation of the received data 101 (where N is an even number), it is judged that a data of value V is continuously received (N/2) times.